



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/535,598	11/28/2005	Adrian Traskov	AP10578	7490
7590 Gerlinde M Nattler Continental Teves Inc One Continental Drive Auburn Hills, MI 48326		01/11/2007	EXAMINER DUNCAN, MARC M	
			ART UNIT 2113	PAPER NUMBER
SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE		
3 MONTHS	01/11/2007	PAPER		

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)
	10/535,598	TRASKOV ET AL.
	Examiner Marc Duncan	Art Unit 2113

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 28 November 2005.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 21-40 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 21,22,28-37 and 39 is/are rejected.
- 7) Claim(s) 23-27,38 and 40 is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 19 May 2005 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) Notice of Informal Patent Application
- 6) Other: _____.

DETAILED ACTION

Status of the Claims

Claims 21-22, 28-29, 32-33 and 39 are rejected under 35 U.S.C. 102(e) as being anticipated by Moyer et al. (6,769,076).

Claims 21-22, 28-29 and 32-37 are rejected under 35 U.S.C. 102(e) as being anticipated by Corti et al. (6,834,360).

Claims 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moyer in view of Madduri (6,142,683).

Claims 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Corti in view of Madduri (6,142,683).

Claims 23-27, 38 and 40 are objected to.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 21-22, 28-29, 32-33 and 39 are rejected under 35 U.S.C. 102(e) as being anticipated by Moyer et al. (6,769,076).

Regarding claim 21:

Moyer teaches:

a CPU (Fig. 1);

a CPU bus (Fig. 1);

a memory (Fig. 1 and col. 8 lines 36-40); and

at least one communication module for input or output of analysis data by way of a test interface (Fig. 1 – 105), wherein the communication module permits the memory and input and output access operations of the embedded system to be monitored and/or logged without using clock cycles of the CPU (col. 2 line 66-col. 3 line 1 and col. 3 lines 9-11).

Regarding claim 22:

Moyer teaches:

wherein at least three freely selectable analysis modes, with the analysis modes, in the way and extent of participation of the CPU, differing from each other in the read and/or write operations of data for analyzing purposes (col. 4 lines 60-65).

Regarding claim 28:

Moyer teaches:

wherein the communication module is integrated into the embedded system (Fig. 1).

Regarding claim 29:

Moyer teaches:

wherein the test interface is connected to a test code memory arranged outside the embedded system (col. 4 lines 50-57 – the workstation necessarily includes a memory as part of the necessary hardware. This memory is equivalent to the test code memory of the instant claims).

Regarding claim 32:

See the teachings of claim 21 above.

Regarding claim 33:

Claim 33 is rejected as the method of using the apparatus of claim 21.

Regarding claim 39:

Moyer teaches:

wherein a mode of the embedded system is provided in which all write and/or read access operations of the CPU are rerouted to the communication module (col. 4 lines 60-65).

Claims 21-22, 28-29 and 32-37 are rejected under 35 U.S.C. 102(e) as being anticipated by Corti et al. (6,834,360).

Regarding claim 21:

Corti teaches:

a CPU (Fig. 2);

a CPU bus (Fig. 2);

a memory (col. 3 lines 30-33); and

at least one communication module for input or output of analysis data by way of a test interface, wherein the communication module permits the memory and input and output access operations of the embedded system to be monitored and/or logged without using clock cycles of the CPU (col. 2 lines 43-48).

Regarding claim 22:

Corti teaches:

wherein at least three freely selectable analysis modes, with the analysis modes, in the way and extent of participation of the CPU, differing from each other in the read and/or write operations of data for analyzing purposes (col. 6 lines 24-29).

Regarding claim 28:

Corti teaches:

wherein the communication module is integrated into the embedded system (Fig. 2).

Regarding claim 29:

Corti teaches:

wherein the test interface is connected to a test code memory arranged outside the embedded system (col. 4 lines 30-33).

Regarding claim 32:

See the teachings concerning claim 21 above.

Regarding claim 33:

Claim 33 is rejected as the method of using the apparatus of claim 21.

Regarding claim 34:

Corti teaches:

wherein the memory content or a correspondingly assessable information of the embedded system, in whole or in part, is copied in real time into an external memory, with the data being buffered in particular before this operation (col. 3 lines 36-40),

and/or the data content of an external memory or a correspondingly assessable information about the memory content of the memory, in whole or in part, is copied in real time into a memory of the embedded system, with the data being buffered in particular before this operation (col. 4 lines 30-33).

Regarding claim 35:

Corti teaches:

wherein the external memory is used to transmit data for typical debugging applications (col. 4 lines 30-33).

Regarding claim 36:

Corti teaches:

wherein only the data needed for debugging is transferred to the external memory in the event of access operations of the CPU to RAM (col. 5 lines 1-10).

Regarding claim 37:

Corti teaches:

wherein at least the write access operations or the read access operations of the CPU are logged by means of a buffer store (col. 3 lines 55-61).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

Art Unit: 2113

2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moyer in view of Madduri (6,142,683).

Regarding claim 30:

The teachings of Moyer are outlined above.

Moyer does not explicitly teach transferring data to external memory using a parallel interface. Moyer does, however, teach transferring data to external memory.

Madduri teaches transferring data to external memory using a parallel interface (col. 3 lines 23-27).

It would have been obvious to one of ordinary skill in the art at the time of invention to combine the parallel interface of Madduri with the external data transfer of Moyer.

One of ordinary skill in the art would have been motivated to make the combination because Madduri teaches that the use of the parallel interface provides higher speed access (col. 5 lines 50-53).

Regarding claim 31:

Moyer teaches:

wherein the external memory is connected to a data conditioning device providing an interface connection to external debugging applications (col. 4 lines 50-57).

Claims 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Corti in view of Madduri (6,142,683).

Regarding claim 30:

The teachings of Corti are outlined above.

Corti does not explicitly teach transferring data to external memory using a parallel interface. Corti does, however, teach transferring data to external memory.

Madduri teaches transferring data to external memory using a parallel interface (col. 3 lines 23-27).

It would have been obvious to one of ordinary skill in the art at the time of invention to combine the parallel interface of Madduri with the external data transfer of Corti.

One of ordinary skill in the art would have been motivated to make the combination because Madduri teaches that the use of the parallel interface provides higher speed access (col. 5 lines 50-53).

Regarding claim 31:

Corti teaches:

wherein the external memory is connected to a data conditioning device providing an interface connection to external debugging applications (col. 4 lines 30-35).

Allowable Subject Matter

Claims 23-27, 38 and 40 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Prior art was not found that explicitly teaches or fairly suggests direct reading and writing of the CPU out of/into an external memory is executed by using clock cycles as outlined in claim 23. Prior art was not found that explicitly teaches or fairly suggests wherein information about the write access operations is written without additional CPU commands into the buffer store or directly into the communication module, and the information about the read access operations is written into the buffer store with active assistance of the CPU as outlined in claim 38. Prior art was not found that explicitly teaches or fairly suggests a mode of the embedded system is provided in which only either the write access operations or the read access operations of the CPU are rerouted to the communication module, and the other access operations of the CPU to the memory are logged actively by the CPU into the external memory as outlined in claim 40. These limitations are considered allowable only in combination with all limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marc Duncan whose telephone number is 571-272-3646. The examiner can normally be reached on M-F 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on 571-272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



md

A handwritten signature in black ink, appearing to read "Marc" followed by a surname starting with "D". Below the signature, the initials "md" are handwritten.